REMARKS

Claims 1-11 and 14-22 are pending in the application.

Claims 1-3, 6, 7, 9-11 and 14-19 have been rejected.

Claims 4, 5, 8 and 20 are objected to.

Claims 21 and 22 are allowed.

Claims 3, 8, 20, and 22 have been amended to correct minor typographical errors. The scope of these claims has not been narrowed by the amendments. Claims 23 and 24 have been added. No new matter has been added by these amendments and additions.

Rejection of Claims under 35 U.S.C. § 103

Claims 1-3, 6, 7, 9-11 and 14-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa (U.S. Pat. No. 5,748,018) (hereinafter referred to as "Ishikawa") in view of Cannella, Jr. (U.S. Pat. No. 5,668,810) (hereinafter referred to as "Cannella"). Applicants respectfully traverse this rejection.

The Office Action relies on Ishikawa to teach "a source clock domain in a first network protocol layer, comprising: a register having a first input for receiving a data signal, a second input for receiving a clock signal, and an output; and a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register," as recited in claim 1. Office Action, p. 2.

As noted by Applicants in their previous responses (mailed February 20, 2004 and January 19, 2005), at col. 4, lines 14-33, Ishikawa recites:

> Referring to FIG. 2B, there is shown a timing chart illustrating an operation of the data output circuit shown in FIG. 2A. In addition, "assuming that an internal delay time of the D-FF 101 as compared with the external clock signal CLK is t_q, and a delay time of the output buffer 102 as compared with the output of the D-FF 101 is t_b, a delay time t_d in the data transfer as compared with the external clock CLK is expressed as $t_q + t_b$. On the other hand, assuming that a difference in time between the external clock signal CLK and the delayed clock signal CLKD is t_b, a

> delay time t_D in the data transfer as compared with the delayed clock CLKD is expressed as follows:
>
> $t_D = t_q + t_b - t_b = t_q$
>
> Accordingly, the delay time t_D in the data transfer becomes equal to t_q, and therefore, this becomes substantially equivalent to the fact that the internal clock signal is advanced as compared with the external clock by the time t_b by using the PLL circuit.

Ishikawa also teaches that the data transfer can be executed within Tcycle "if the delay time t_{B103} of the output buffer 103 is set to a value not smaller than $\{t_s + t_q + t_b - Tcycle\}$". Ishikawa, col. 5, lines 14-28. Accordingly, Ishikawa neither teaches nor suggests making the delay of buffer 103 (which the Examiner relies on to teach the "buffer" of claim 1) substantially equivalent to the delay of D-FF 101 (which the Examiner relies on to teach the "register" of claim 1).

The current Office Action (mailed June 23, 2005) also relies upon the timing diagram shown in FIG. 3B of Ishikawa to show that "the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D". As with FIG. 2B, FIG. 3B is not drawn to any particular scale, and thus Applicants assert that any apparent similarities would not have suggested anything to one of ordinary skill in the art, especially given that no other portion of the reference teaches or suggests such similarities. Furthermore, even assuming that FIG. 3B is drawn to scale, the quantity labeled t_{B103} is perceptively smaller (1.25 cm in Applicants' copy of the reference) than the quantity labeled t_D (1.5 cm in Applicants' copy of the reference). Given that the scale of the drawing is not labeled, the drawing does not show the quantities as being the same size, and no other teaching or suggestion that these quantities are "substantially equal" has been provided, Applicants assert that the reference, both alone and in combination with Cannella, simply does not teach or suggest this feature of claim 1.

For at least the foregoing reasons, claim 1 is patentable over the cited art, as are dependent claims 2-3, 6, 7, and 9-11. Claims 14-19 are patentable over the cited art for similar reasons.

Further with respect to claim 1, there is no suggestion to combine Ishikawa and Cannella. "To support the conclusion that the claimed combination is directed to obvious

subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references... [S]implicity and hindsight are not the proper criteria for resolving the issue of obviousness." *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Int'f 1985).

On page 3, the Office Action states that "it would have been obvious... to implement a link layer and a physical layer in an IC circuit as taught by Cannella since such implementation is well known in the art in designing network communication equipments." The Office Action has not cited any express or implied suggestions to make the asserted combination within the references. Applicants note that the references themselves do not provide any suggestion to make the asserted combination. As noted in previous responses, the circuits taught in Ishikawa are clearly not implementing network protocol layers (in fact, none of the terms "network", "layer", or "protocol" are used in Ishikawa). Thus, Ishikawa cannot reasonably be read as teaching or suggesting that its circuits be used as network protocol layers. Similarly, the cited portions of Cannella do not teach or suggest that it would be desirable to implement the features of Ishikawa's circuits within an integrated circuit that implements a network protocol layer. The references simply do not suggest that it would be desirable to combine the features of Ishikawa's circuit with the features of Cannella's circuit. Accordingly, no reference has been cited in support of the asserted suggestion to combine Ishikawa and Cannella.

The Office Action also does not show a convincing line of reasoning as to why one of ordinary skill in the art would combine the references. Instead, the Office Action appears to be basing its suggestion to combine on the fact that such a modification would have been within the capabilities of one of ordinary skill in the art ("since such implementation is well known in the art in designing network communication equipments," Office Action, p. 3). While it is conceivable that one skilled in the art, after receiving instructions to design a system that has the features of Applicants' claims, would be capable of designing such a system, there is nothing in the statutes or the case law which makes that which is within the capabilities of one skilled in the art synonymous with obviousness. *See Ex parte Gerlach and Woerner*, 212 U.S.P.Q. 471.

Furthermore, the Board has held that examiners have misstated the law by "equating that which is within the capabilities of the skilled designer with obviousness." *In re Sung Nam Cho,* 813 F.2d 378. For at least the foregoing reasons, the obviousness rejection is improper. Applicants respectfully request the withdrawal of this rejection.

Objections

Claims 4, 5, 8, and 20 were objected to as being dependent upon a rejected base claim. Applicants note that claims 5 and 8, which respectively depend on claims 21 and 5, are not dependent upon rejected base claims. Accordingly, Applicants assert that these claims are allowable. Claims 4 and 20 are believed to be allowable for at least the reasons presented above with respect to claim 1.

Allowed Claims

Claims 21 and 22 are identified as being allowed. Applicants thank the Examiner for the thoughtful consideration of these claims.

New Claims

Claims 23 and 24 are patentable over the cited art for at least the reasons presented above with respect to claim 1.

CONCLUSION

In view of the amendments and remarks set forth herein, the application and the claims therein are believed to be in condition for allowance without any further examination and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on Sept. 23, 2005.

Brenna A Brock 9/23/2005
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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